Building Heterogeneous Chiplets with AMBA Interconnects

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Building Heterogeneous Chiplets with AMBA Interconnects

- The scalable AMBA CHI (Coherent Hub Interface) specification has provided the foundation for building complex SoCs across a broad range of applications including mobile, networking, automotive and data centers. The high-speed, credited, packetized attributes make it well suited to build multi-chip(let) networks.

- This talk will highlight the scope of a new AMBA CHI Chip-to-Chip specification that is currently in development and illustrate how the specification will complement chiplet standards such as UCIe.

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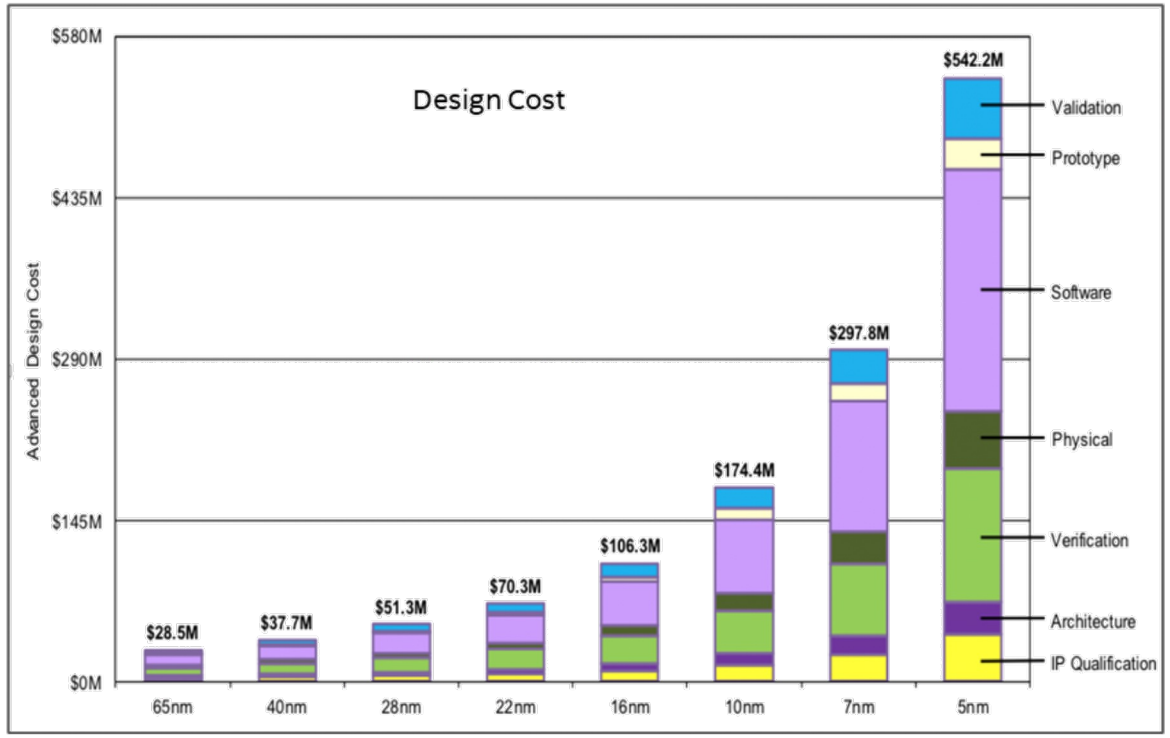
Economics Driving Chiplet Investments

- Increasing design cost with less benefit
  - Logic continues to scale, but IO & SRAM only shrinking by 5~10%
- SoC NRE limiting product derivatives
  - Chiplets lowers overall platform cost and barrier to deploy a diverse product portfolio
- Market demands performance and efficiency
  - New chiplet technology offers a 20x speed and power improvement over traditional PCIe SERDES



Source: IBS, as cited in IEEE Heterogeneous Integration Roadmap

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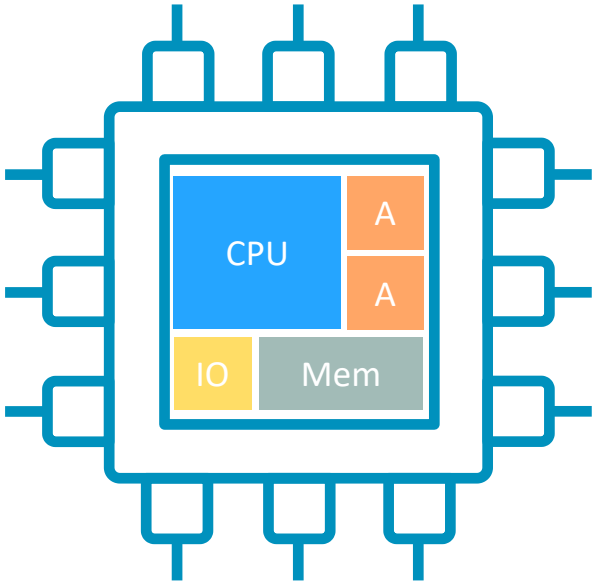
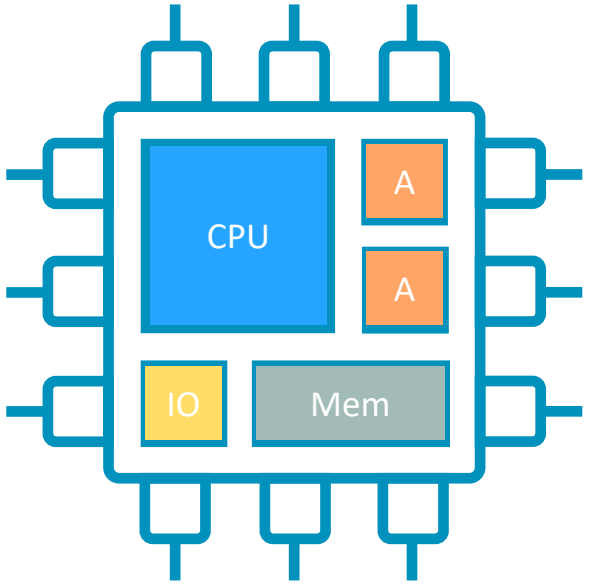
SoC Accelerator Framework for Heterogenous Compute

Moving from Monolithic to Chiplet

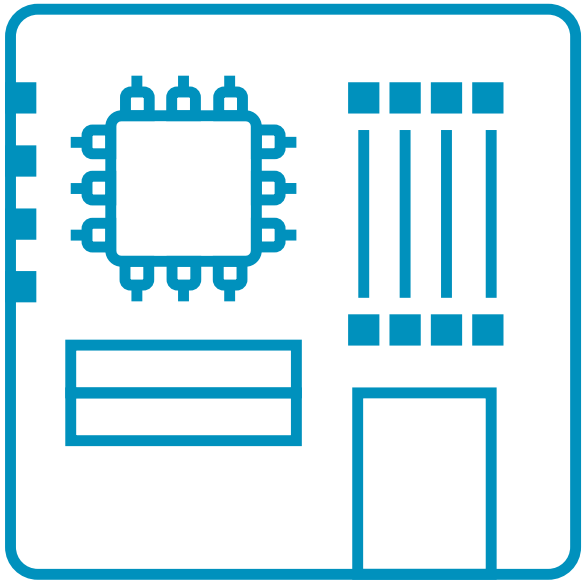
SINGLE DIE
(AMBA)



MULTI-DIE
(UCIe)



MULTI-CHIP on
PCB
(PCIe, CXL)



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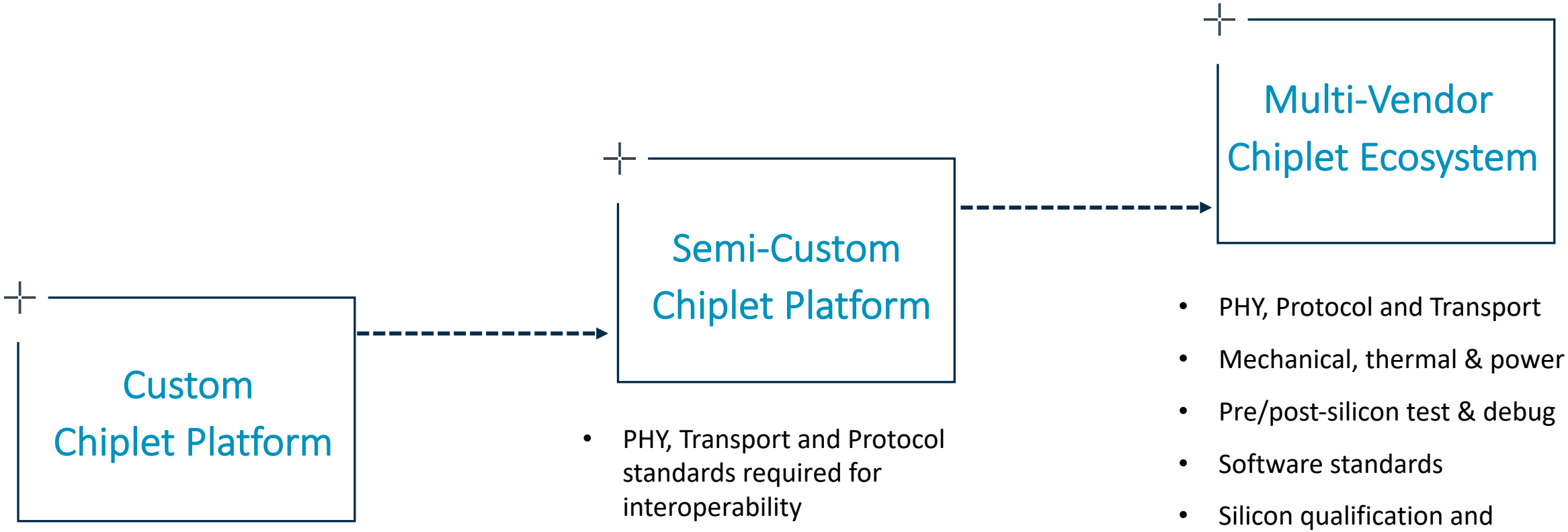
The Path to a Chiplet Ecosystem



- PHY, Transport and Protocol standards drive IP development and broader adoption

- PHY, Transport and Protocol standards required for interoperability

- PHY, Protocol and Transport
- Mechanical, thermal & power
- Pre/post-silicon test & debug
- Software standards
- Silicon qualification and reliability

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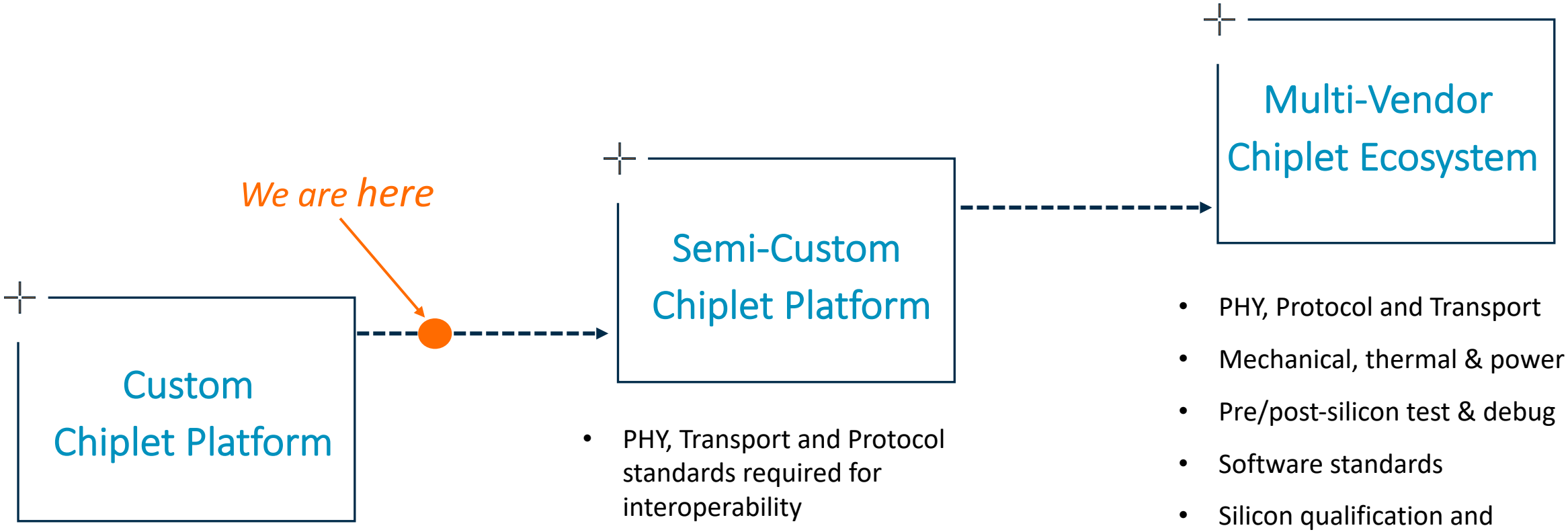
The Path to a Chiplet Ecosystem



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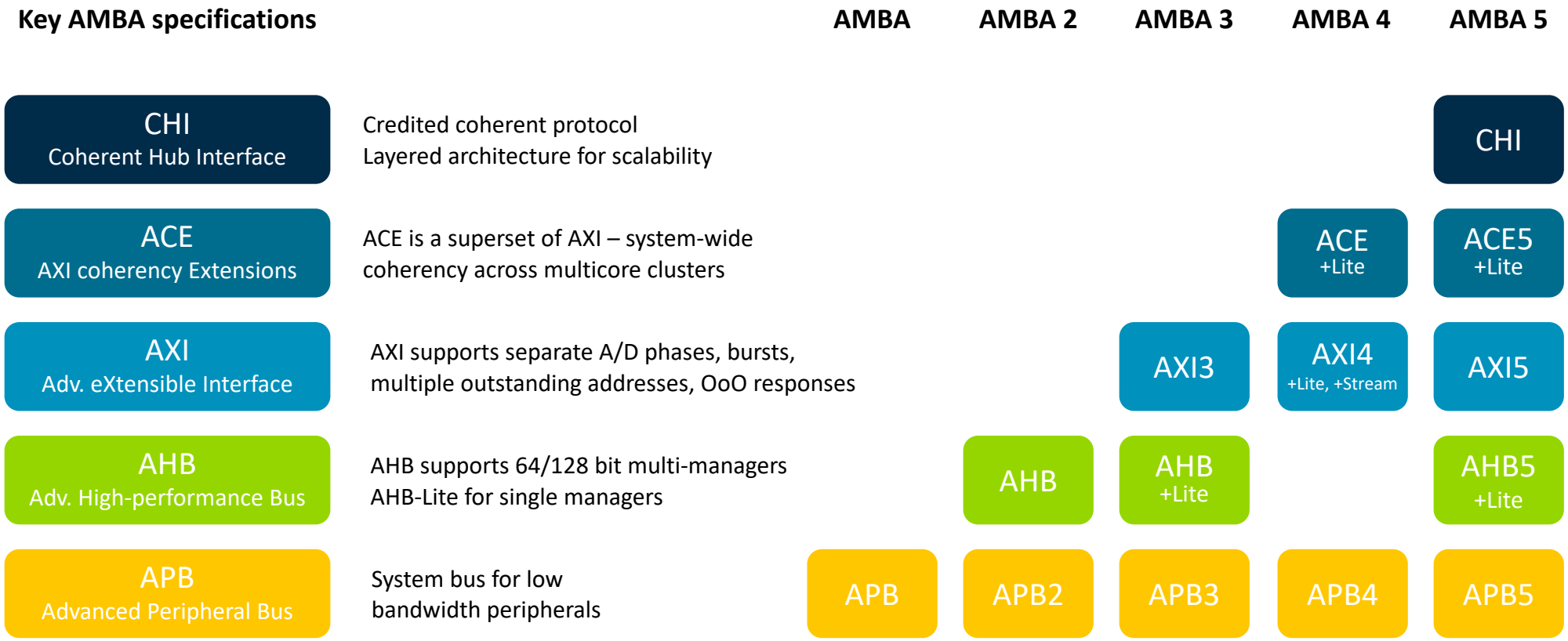
AMBA: Specifications, Interface and Protocols Diagram

Key AMBA Specifications: CHI, ACE, AXI, AHB, APB



Selected AMBA specifications only. Other specifications include: ATB, ATP, CXS, DTI, GFB, LPI and LTI.

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AMBA: Specifications, Interface and Protocols Diagram

Key AMBA Specifications: CHI, ACE, AXI, AHB, APB

Key AMBA specifications		AMBA	AMBA 2	AMBA 3	AMBA 4	AMBA 5
CHI Coherent Hub Interface	**Credited coherent protocol** **Layered architecture for scalability**					CHI
ACE AXI coherency Extensions	ACE is a superset of AXI – system-wide coherency across multicore clusters				ACE +Lite	ACE5 +Lite
AXI Adv. eXtensible Interface	AXI supports separate A/D phases, bursts, multiple outstanding addresses, OoO responses			AXI3	AXI4 +Lite, +Stream	AXI5
AHB Adv. High-performance Bus	AHB supports 64/128 bit multi-managers AHB-Lite for single managers		AHB	AHB +Lite		AHB5 +Lite
APB Advanced Peripheral Bus	System bus for low bandwidth peripherals	APB	APB2	APB3	APB4	APB5

Selected AMBA specifications only. Other specifications include: ATB, ATP, CXS, DTI, GFB, LPI and LTI.

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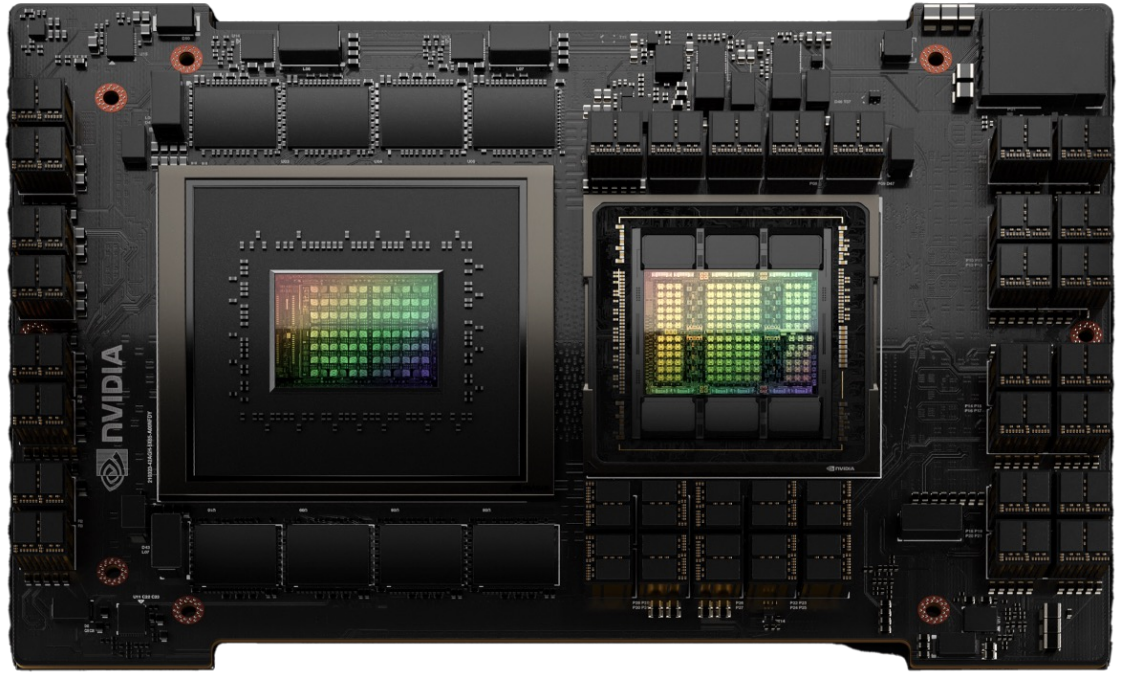
NVIDIA Grace Hopper Superchip

- Combining Grace CPU (72x Arm Neoverse V2 CPUs) with Hopper GPU inside the package
- New 900 GB/s NVIDIA-CTC interconnect using AMBA CHI for the multichip protocol
- Unified virtual memory system with shared paged tables
- 30X Higher System Memory B/W to GPU in a Server

Grace Hopper Superchip



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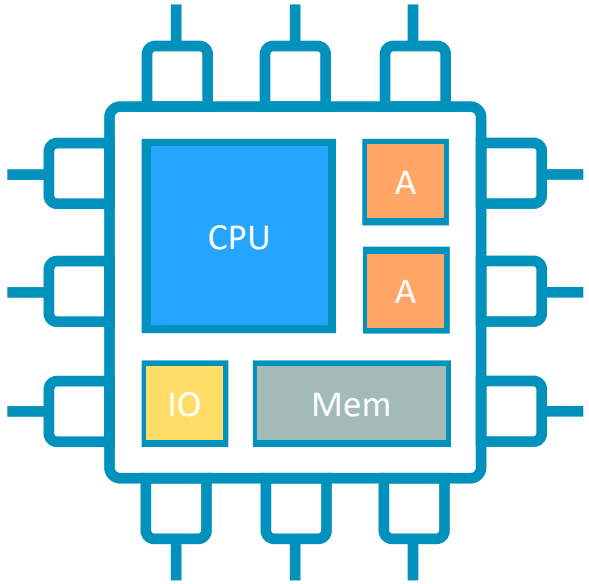
Extending AMBA Architecture to Multichip with CHI C2C



Accelerator

Memory (DDR, HBM, etc)

IO (PCIe, CXL, etc)

- New AMBA CHI Chip-to-Chip Specification in Development
  - A unified interface for device attach
    - Compute, Accelerator and Memory
    - Coherent and IO Coherent accelerator traffic
  - Architectural features extended across chip(let) boundaries
    - Virtualization (DVM), Interrupts, Timers
    - Telemetry and Resource Management
    - Security for trust, memory protection and Confidential Compute
  - Composable with die re-use across different solutions
    - Appropriate for Multi-Die and Multi-chip through PCB
    - Supports UCIe and bespoke PHY options

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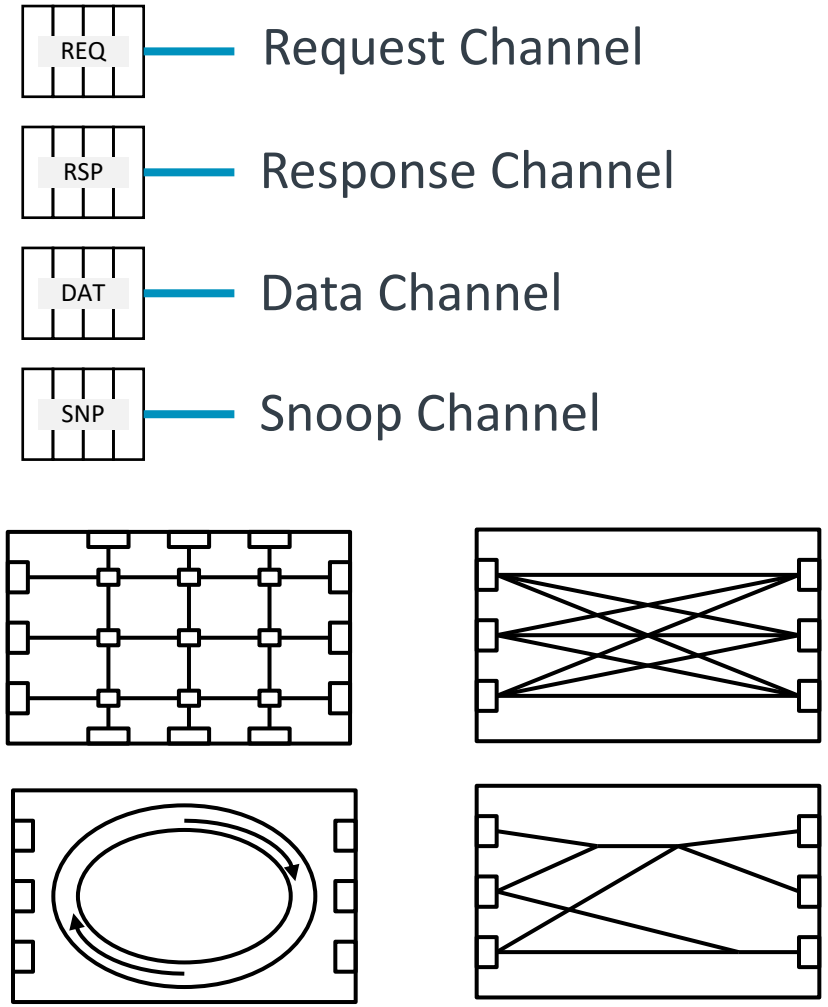
CHI Protocol Overview

- AMBA 5 CHI protocol features:
  - Full cache coherency model
  - Supports snoop filter and directory-based systems for snoop scaling
  - Definition for simpler IO and Memory interfaces
- Other features:
  - Credited, non-blocking, high-speed transports
  - Configurable bus width - 128, 256 or 512 bits
  - Support for end-to-end *Quality of Service* (QoS)
  - Virtual memory management through *Distributed Virtual Memory* (DVM) operations

AMBA CHI Specification:
https://developer.arm.com/search#q=amba%205%20chi%20architecture%20specification



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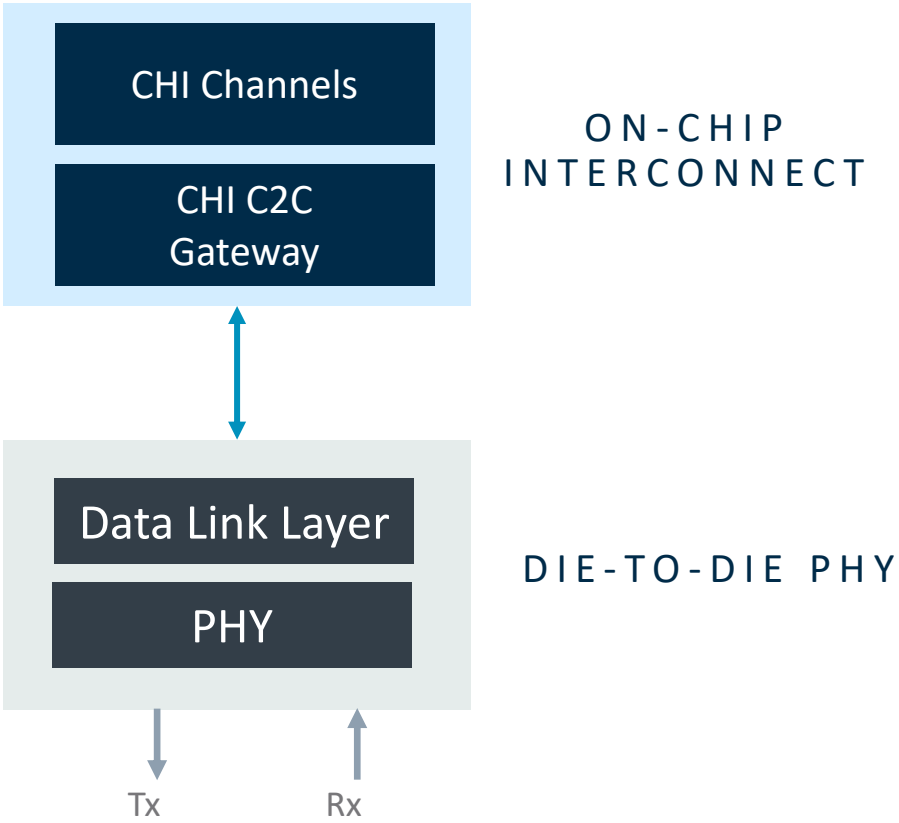
AMBA CHI Chip-to-Chip Specification

- Packetization of CHI channels with cross-chip credit exchange
- Link aggregation for bandwidth scalability
- Portability across different PHY and packaging technology
- Clean interface definition between on-chip interconnect and PHY/Link Layer for IP portability between vendors
- Support for point-to-point and chiplet network topologies



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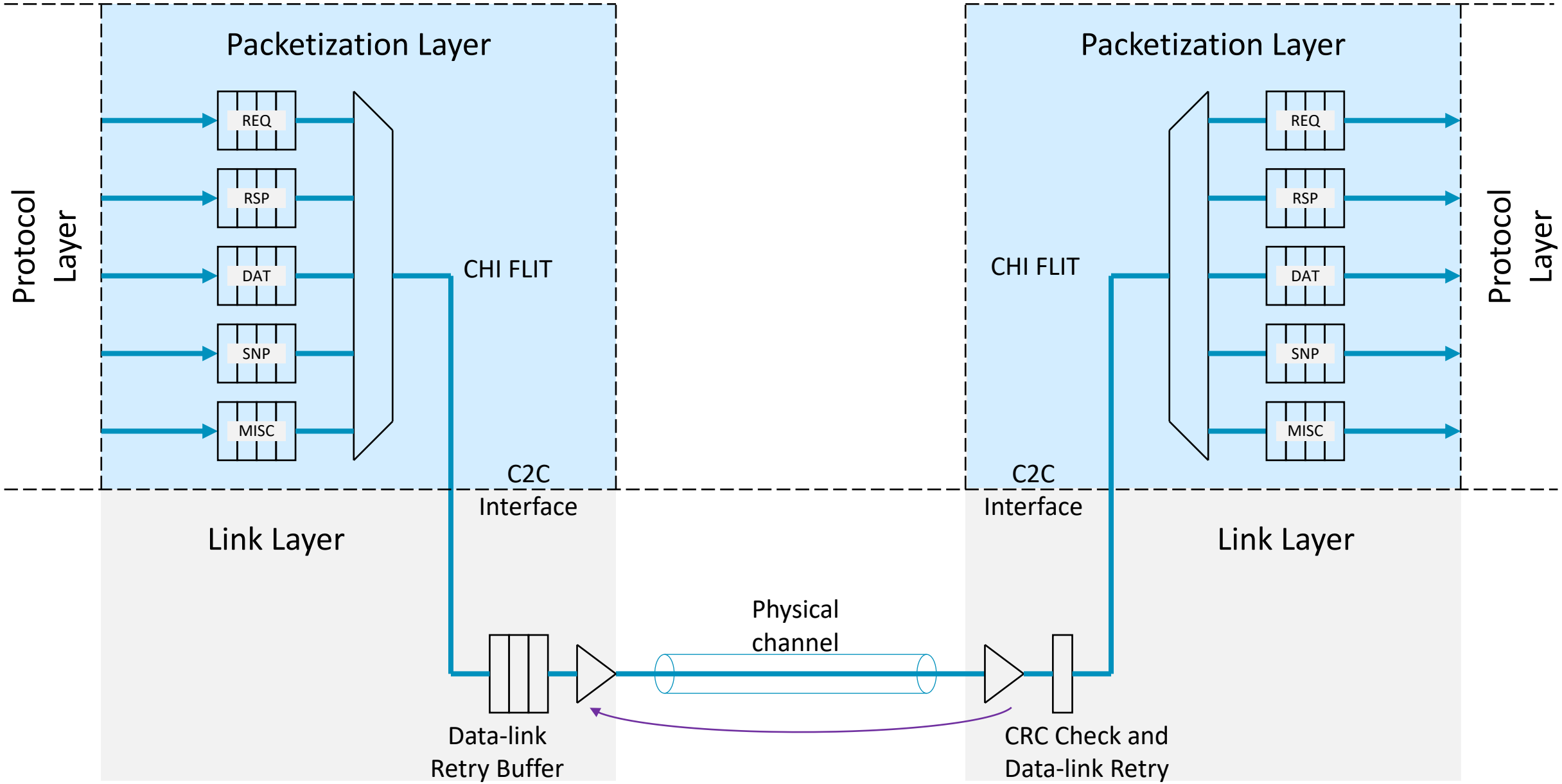
Packetization Layer
REQ
RSP
DAT
SNP
MISC
Protocol Layer
CHI FLIT
C2C Interface
Link Layer
Physical channel
Data-link Retry Buffer
CRC Check and Data-link Retry
Packetization Layer
REQ
RSP
DAT
SNP
MISC
CHI FLIT
C2C Interface
Link Layer
Protocol Layer

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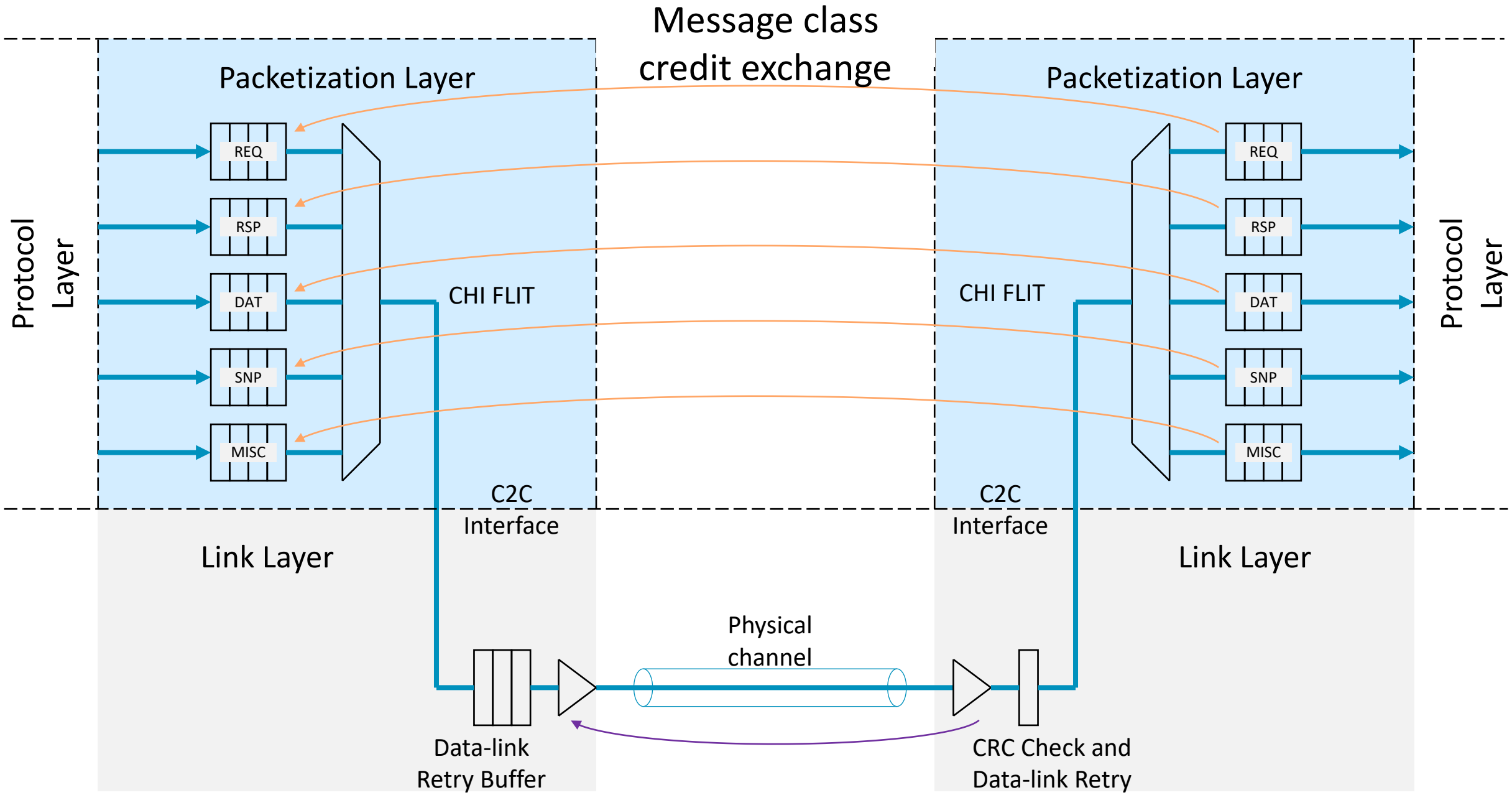
Message class
credit exchange
Packetization Layer
Packetization Layer
Protocol Layer
Protocol Layer
REQ
RSP
DAT
SNP
MISC
REQ
RSP
DAT
SNP
MISC
CHI FLIT
CHI FLIT
C2C
Interface
C2C
Interface
Link Layer
Link Layer
Physical
channel
Data-link
Retry Buffer
CRC Check and
Data-link Retry

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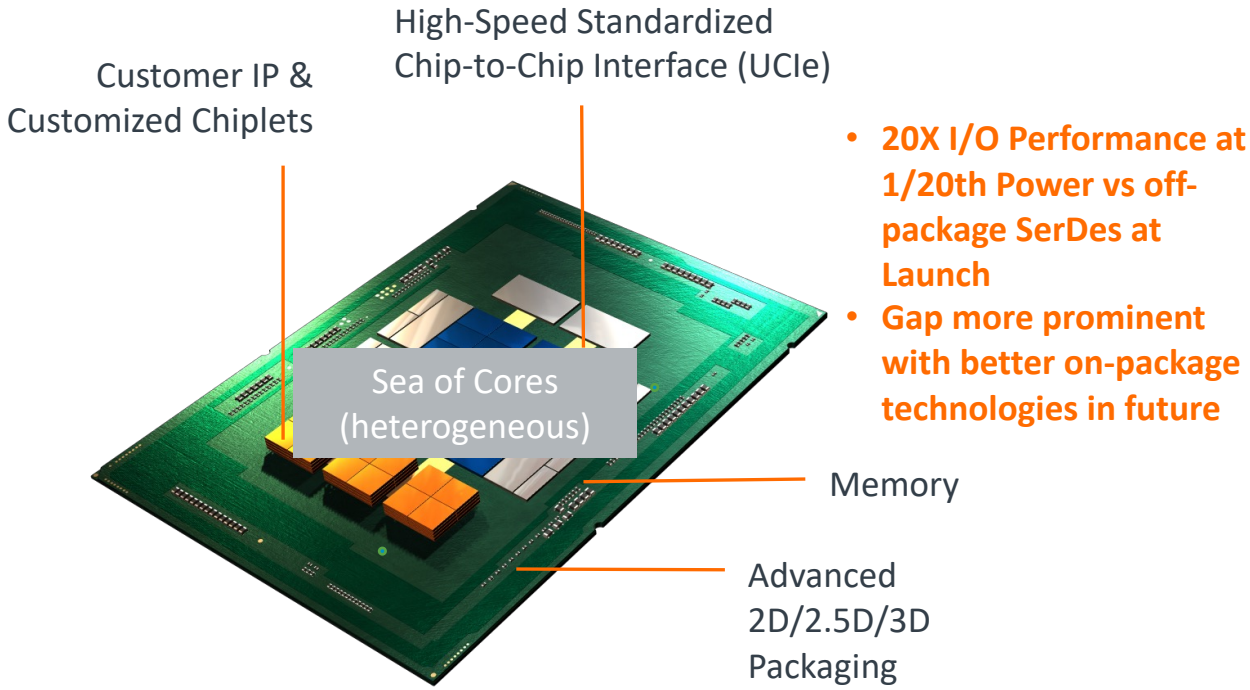
Open Chiplet: Platform on a Package

UCIe Universal Chiplet Interconnect Express

Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)



- **20X I/O Performance at 1/20th Power vs off-package SerDes at Launch**
- **Gap more prominent with better on-package technologies in future**

Heterogeneous Integration Fueled by an Open Chiplet Ecosystem (Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

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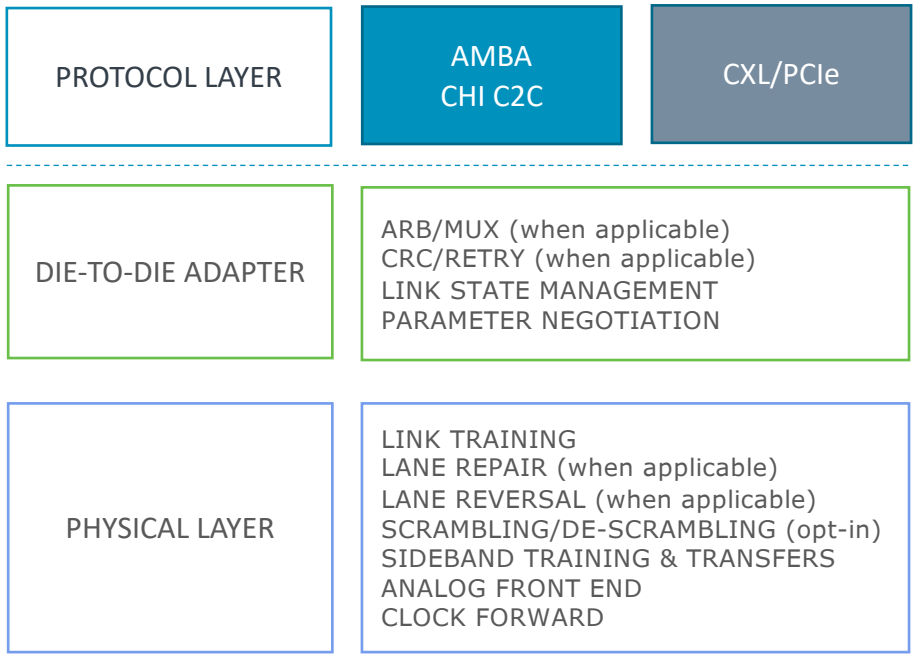
UCIe Layered Architecture

- UCIe 1.0 provides a complete multichip interface specification
  - Leverages PCIe/CXL protocol for architectural agnostic attach
  - PHY definitions for 2.1D and 2.5D packaging
- AMBA CHI C2C will use the UCIe Streaming Interface
  - Streaming interface with additional flit formats provide link robustness using UCIe defined data-link CRC and retry
- Arm will support both CHI and CXL/PCIe options to provide flexibility for the wide range of potential chiplet integrations
- UCIe defines support for both 2.1D and 2.5D packaging

https://www.uciexpress.org/webinars



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AMBA CHI C2C Extends on-chip performance to Multi-chip(lets)

- Economics are driving chiplet investments and momentum toward Semi-Custom Chiplet Platforms
  - Standards investments for PHY, Transport and Protocol IP accessibility and interoperability
  - New PHY and packaging technology offering ‘on-chip’ performance and efficiency; 20x speed and power improvement over traditional PCIe SERDES

- New AMBA CHI Chip-to-Chip specification will extend the on-chip bus to multi-chip
  - Provides a unified memory, security and virtualization architecture across chiplets
  - Built to run over standards based die-to-die interconnects such as UCIe or bespoke solutions

- Stay tuned!
  - AMBA CHI C2C specification is under development, more updates expected throughout the year

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Thank You
Danke
Gracias
Grazie
谢谢
ありがとう
Asante
Merci
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Kiitos
شكرًا
ধন্যবাদ
תודה

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